

# Design of Mixed Signal FSM Sequence Detector with CMOS Inverter

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**Abstract**—An FSM is an abstract machine that can exist in only one of a finite number of states at a time. A Moore FSM is one which depends only on the value of present state and not the value of input. A sequence detector is a circuit that takes an input string of bits and generates an output 'HIGH' when the target sequence has been detected. Analog input from a CMOS inverter is fed into this digital block and output is observed.

**Keywords**—CMOS Inverter, Finite State Machine, Mixed Signals, Moore FSM, Sequence Detector

## REFERENCE CIRCUIT DETAILS

In this paper, a Finite State Machine based sequence detector is proposed. This is a Moore based FSM, where the output is only dependent on the present state. This FSM block is a digital block consisting of three inputs, which are clock, sequence\_in and reset. It has one output, the detector\_out. This is coded in Verilog.

For the analog part, a CMOS inverter is implemented using MOS transistors. The voltage is supplied to the CMOS inverter. The output of the inverter is fed into an ADC block (Analog-to-Digital). The output from this block is passed as input to the FSM digital block along with additional voltage supplies for the clock and reset. The output of the FSM block will be a single output which goes high when the required sequence is detected.

The CMOS inverter will be made up of pmos and nmos as shown in Fig.1. The FSM to be implemented will be a 1011 sequence detector. When this particular sequence is detected, the detector\_out will show an output of 1. This is passed through a DAC block (Digital-to-Analog), from which the output voltage is measured.

## REFERENCE CIRCUIT DESIGN

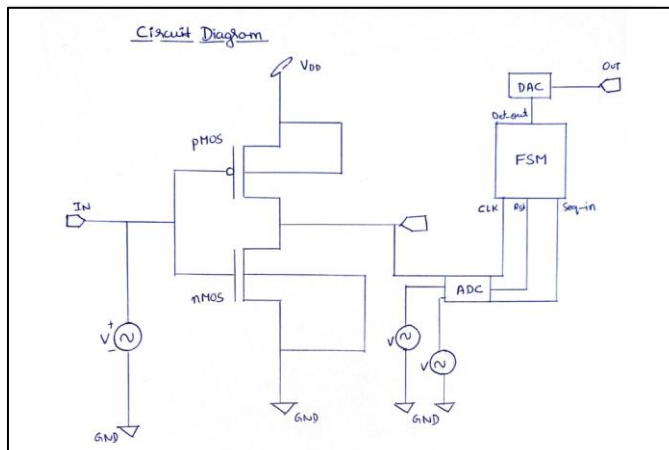


Fig.1

## REFERENCE CIRCUIT WAVEFORMS

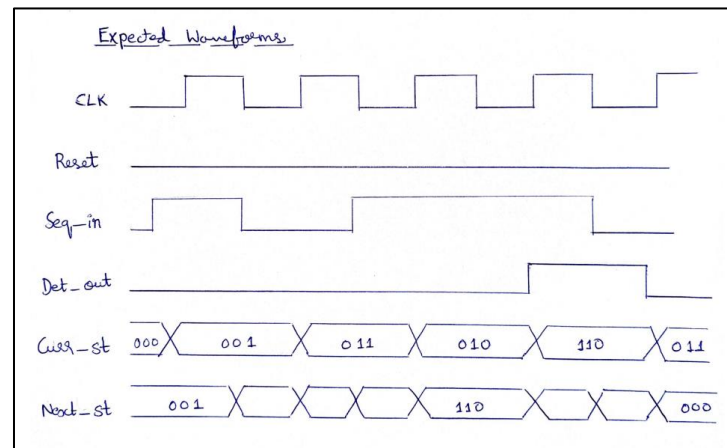


Fig.2

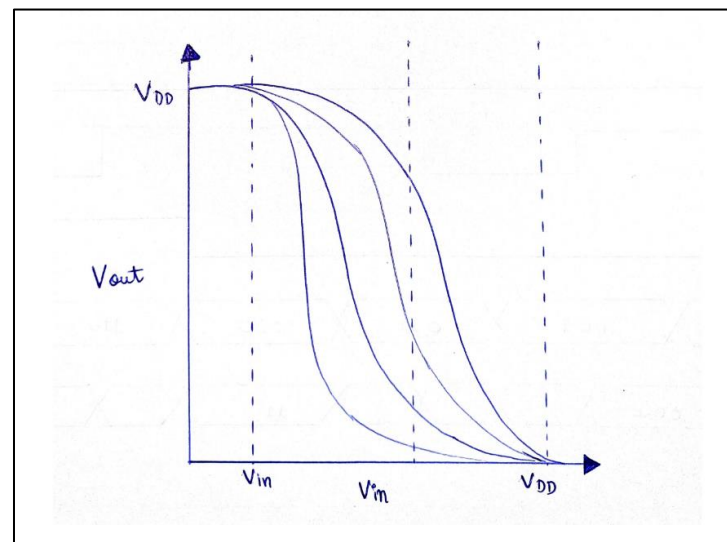


Fig.3

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